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SLIM SPACER DEVICE AND MANUFACTURING METHOD

FIELD OF THE INVENTION

001 This invention generally relates to processes for forming semiconductor devices including CMOS and MOSFET devices and more particularly to a CMOS device and method for forming the same having a Slim spacer with improved electrical performance including reduced short channel effects and increased charge carrier mobility.

BACKGROUND OF THE INVENTION

002 As MOSFET and CMOS device characteristic sizes are scaled below 0.25 microns including below 0.1 micron, the device designs need to be modified for each generation of device scaling down. For example, short channel effects (SCE) are one of the most important challenges for designers to overcome as device critical dimensions are scaled down. Among the many manifestations of SCE, are Voltage threshold (V_T) rolloff, drain induced barrier lowering (DIBL), and subthreshold swing variation.

003 Source/Drain (S/D) junction depth and channel doping are some of the few parameters that can be changed to reduce SCE. Since the source drain extension (SDE) implants are self-aligned

to the gate edge, the junction depth of the S/D regions is typically scaled to the gate length (L_G). One problem with reducing junction depth is the effect of increasing the S/D region sheet resistance, which reduces drive current (I_D).

004 One approach to reducing the increase in S/D sheet resistance with shallower junction depths is to form salicides over the S/D regions. However, the width of spacers which mask an underlying lightly doped regions also referred to as source drain extension (SDE) regions during a S/D implant process have the effect of reducing the amount of salicide that may be formed over the S/D and SDE regions. Therefore, while it may be desirable to have a desired spacer width and a desired underlying SDE region width, the spacer width limits the degree of lowering the sheet resistance of the S/D region by salicide formation leading to lower drive current (I_D).

005 In addition, as gate lengths become smaller, for example less than about 80 nanometers, conventional processes for forming spacers are no longer adequate to precisely position the S/D implant regions, thereby leading to increased SCE. In some approaches in the prior art, disposable spacers have been proposed to address the problem of having a desirable spacer width to form a desired S/D region and subsequent salicide width to lower S/D region sheet resistance. Among the shortcomings of disposable spacers includes costly and complicated processes requiring extra process steps which undesirably decreases throughput and adds to cost. In addition, disposable spacers lead to reduced control in forming a selected level of tensile or compressive stresses in the channel region to achieve improved charge mobility.

006 There is therefore a need in the semiconductor integrated circuit manufacturing art for an improved method for forming dielectric spacers to achieve desired dimensions while reducing S/D region electrical resistance and associated SCE effects while increasing charge mobility at acceptable process throughput and process cost.

007 It is therefore among the objects of the present invention to provide an improved method for forming dielectric spacers to achieve desired dimensions while reducing S/D region electrical resistance and associated SCE effects while increasing charge mobility at acceptable process throughput and process cost, as well as overcoming other shortcomings of the prior art.

008 In another approach, strain in the channel is introduced after the transistor is formed. In this approach, a high stress film is formed over a completed transistor structure formed in a silicon substrate. The high stress film or stressor exerts significant influence on the channel, modifying the silicon lattice spacing in the channel region, and thus introducing strain in the channel region. In this case, the stressor is placed above the completed transistor structure. This scheme is described in detail in a paper by A. Shimizu et al., entitled "Local mechanical stress control (LMC): a new technique for CMOS performance enhancement," published in pp. 433-436 of the Digest of Technical Papers of the 2001 International Electron Device Meeting, which is incorporated herein by reference.

SUMMARY OF THE INVENTION

009 To achieve the foregoing and other objects, and in accordance with the purposes of the present invention, as embodied and broadly described herein, the present invention provides a CMOS structure comprising a Slim spacer and method for forming the same to reduce an S/D electrical resistance and improve charge mobility in a channel region.

0010 In a first embodiment, the method includes providing a semiconductor substrate including a polysilicon or metal gate structure including at least one overlying hardmask layer; forming spacers selected from the group consisting of oxide/nitride and oxide/nitride oxide layers adjacent the polysilicon or metal gate structure; removing the at least one overlying hardmask layer to expose the polysilicon or metal gate structure; carrying out an ion implant process; carrying out at least one of a wet and dry etching process to reduce the width of the spacers; and, forming at least one dielectric layer over the polysilicon or metal gate structure and spacers in one of tensile and compressive stress.

0011 In one embodiment of the present invention, a semiconductor device is provided on a substrate having a <100> crystal

orientation. Current flow of device is along <100> direction. The mobility of PMOS could be enhanced on this direction.

0012 These and other embodiments, aspects and features of the invention will be better understood from a detailed description of the preferred embodiments of the invention which are further described below in conjunction with the accompanying Figures.

BRIEF DESCRIPTION OF THE DRAWINGS

0013 Figures 1A-1F are cross sectional views including a portion of a gate structure of an exemplary MOSFET showing exemplary manufacturing stages in an integrated circuit manufacturing process according to an embodiment of the present invention.

0014 Figures 2A-2D are cross sectional views including a portion of a gate structure of an exemplary MOSFET showing exemplary manufacturing stages in an integrated circuit manufacturing process according to an embodiment of the present invention.

0015 Figure 3 is a data representation showing the gain in channel stress achieved according to the Slim spacer MOSFET device formed according to embodiments of the present invention.

0016 Figure 4 is a process flow diagram including several embodiments of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

0017 Although the method of the present invention is explained by reference to exemplary device sizes and is most advantageously used with preferred devices sizes, including spacer widths and gate lengths, it will be appreciated that the method of the present invention may be used with other device sizes as well.

0018 Referring to Figures 1A-1F is shown an exemplary implementation of the method of the present invention. Shown are a silicon or silicon germanium substrate 10, an overlying gate dielectric layer (such as oxide) portion 12, and an overlying polysilicon or metal gate electrode portion 14. In an aspect of the invention, at least one hardmask layers are deposited over a polysilicon or metal layer prior to forming the gate structure to form hardmask layer portions 16A and 16B overlying gate electrode portion 14 by conventional deposition, photolithographic and etching processes. For example the lowermost hardmask layer 16A is preferably formed of silicon oxide, e.g., LPCVD or PECVD silicon oxide and hardmask layer 16B is preferably formed of silicon nitride and/or silicon oxynitride by conventional LPCVD

or PECVD processes, for example the two hardmask layer portions 16A and 16B having a total thickness of about 300 Angstroms to about 1000 Angstroms. It will be appreciated that a conventional source/drain extension (SDE) ion implant process may be carried prior to or following removal of the hardmask layer portion 16B to form SDE regions e.g., 20A, 20B as explained below.

0019 Referring to Figure 1B, in an aspect of the invention, the uppermost hardmask layer e.g., 16B is removed by a conventional wet or dry etching process to leave the lowermost hardmask layer portion e.g., 16A overlying the polysilicon or metal electrode portion 14.

0020 Referring to figure 1C, in one embodiment of the invention, an oxide layer, for example LPCVD TEOS oxide is first blanket deposited, for example having a thickness less than about 200 Angstroms, more preferably less than about 150 Angstroms, followed by deposition of a nitride layer, for example silicon nitride or silicon oxynitride (e.g., SiON), preferably silicon nitride, (e.g., Si_3N_4, SiN), preferably by an LPCVD process and preferably having a thickness of greater than about 450 Angstroms. A conventional wet and/or dry etchback process is then carried out to etch through a thickness of the nitride layer

and underlying oxide layer to stop on the hardmask portion 16A to form nitride spacer portion e.g., 18A and oxide spacer portion e.g., 18B adjacent either side of the gate structure.

0021 Referring to Figure 1D, in an important aspect of the invention, a conventional wet or dry etching process, preferably a wet oxide (isotropic) etch process is then carried out, for example using dilute HF and an optional buffer agent, to remove the oxide hardmask layer portion 16A overlying the polysilicon or metal electrode portion 14. It will be appreciated that in an isotropic wet etch process a portion of the oxide spacer portion 18A will be removed as well, preferably to be about co-planar with the polysilicon or metal electrode 14 upper portion, while removing a portion underling the nitride portion 18B. Following removal of the hardmask layer portion 16A overlying the polysilicon or metal electrode portion 14, a conventional S/D ion implantation process, also referred to as a high dose implant (HDI) is then carried out to dope the polysilicon electrode or metal portion 14 as well as form the S/D regions e.g., 22a, 22B adjacent the SDE regions e.g., 20A, 20B.

0022 Referring to Figure 1E, in a critical aspect of the invention, a wet or dry etching process is then carried out to remove a portion of the nitride spacer 18B, to form a Slim

(reduced width) oxide/nitride spacer width from W2 to W1. Advantageously, in the spacer thinning process a portion of the underlying SDE region e.g., 20A is exposed by the reduced width amount e.g., W3. For example, a maximum width W1 of the Slim spacers is preferably less than a width W2 of the SDE doped regions e.g., 20A measured to an edge of the S/D doped region 22A. It will be appreciated that the desired reduction in width of the nitride spacer portion 18B will vary depending on the gate length and the oxide/nitride spacer width W2 present for the S/D implant process prior to thinning, a desired reduction in S/D resistance, and a desired increase in channel stress. Preferably, however, the Slim width W1 of the oxide/nitride spacer 18A and 18B measured from the polysilicon or metal gate electrode sidewall 14, is reduced by greater than about 20 percent of W2 to achieve a desired electrical resistance decrease in S/D region e.g., 22A and SDE region e.g., 20A and/or an increase in channel stress in channel region e.g., 26. In an exemplary embodiment, for a CMOS gate structure having a gate length (L_G), of about 400 Angstroms and a pre-Slim spacer width W2 of about 650 Angstroms, the spacer is reduced to a width W1 of less than about 500 Angstroms, more preferably less than about 350 Angstroms.

0023 Still referring to Figure 1E, following the wet or dry etching process to reduce the spacer width, optionally a salicide formation process is undertaken by conventional processes to form salicide regions e.g., 24A and 24B respectively over the S/D regions e.g., 22A and 22B and a portion of exposed SDE regions e.g., 20A, 20B as well as over the upper portion e.g., 14A of polysilicon electrode 14. Preferably the salicide regions are formed of TiS_2, $CoSi_2$ or NiSi by conventional process of depositing Ti, Co or Ni over exposed silicon and polysilicon or metal portions followed by a subsequent annealing process as is known in the art to form the low resistance phase of the respective salicide. Less preferably, the salicide formation process may be carried out subsequent to the stressed dielectric formation and removal process outlined below.

0024 Advantageously, according to the present invention, by exposure of a portion of the underlying SED regions e.g., 20A in the spacer width reduction process, and subsequent formation of an overlying salicide portion e.g., 24A, the electrical resistance of the S/D regions e.g., 22A and SDE regions e.g., 20A are reduced, thereby allowing reduced gate length and reduced S/D and SDE junction depths to reduced short channel effects (SCE) while increasing the drive current (I_d). For example, the

electrical operating characteristics e.g., I_{Dsat} of MOSFET devices having gate lengths (L_G) of 80 nanometers or less are advantageously improved without accompanying SCE, according to embodiments of the present invention.

0025 Referring to Figure 1F, in a related embodiment of the invention, a stressed dielectric layer 28 in one of tensile or compressive stress is then formed (e.g., blanket deposited) over the gate structure including the S/D regions and SDE regions. For example, the stressed dielectric layer 28 is preferably formed in tensile stress for a NMOS device and preferably formed in compressive stress for a PMOS device. It will be appreciated that the level of the tensile or compressive stress can be varied by a number of factors including the thickness of the stressed dielectric layer 28, preferably being from about 50 Angstroms to about 1000 Angstroms in thickness up to about a 2 GPa respective stress level.

0026 Preferably, the stressed dielectric layer 28 is deposited by a CVD process where the relative reactant flow rates, deposition pressure, and temperature may be varied to vary a composition of the dielectric layer thereby controlling the level of either tensile or compressive stress. For example, stressed dielectric

layer 28 may be a nitride or carbide, such as silicon nitride (e.g., SiN, Si_xN_y), silicon oxynitride (e.g., Si_xON_y), or silicon carbide (e.g., Si_xOC_y) where the stoichiometric proportions x and y may be selected according to CVD process variables as are known in the art to achieve a desired tensile or compressive stress in a deposited dielectric layer. For example, the CVD process may be a low pressure chemical vapor deposition (LPCVD) process, an atomic layer CVD (ALCVD) process, or a plasma enhanced CVD (PECVD) process. The stressed dielectric layer 28 may be removed or left in place following a subsequent annealing process where amorphous portions of the polysilicon are recrystallized thereby increasing a selected stress level on the channel region e.g., 26 to improve carrier mobility.

0027 Referring to Figure 3, advantageously, according to the present invention, the selected amount of stress in the channel region can be increased significantly by reduction of spacer width according to preferred embodiments. For example, shown is a data representation of a CMOS device formed with a reduced spacer width according to embodiments of the present invention. Shown on the vertical axis is a ratio of channel stress to dielectric layer stress (e.g. 28) and on the horizontal axis is shown an spacer width formed according to preferred embodiments.

Data lines A, B and C represent respective spacer widths formed for a CMOS device having respective 25 nm, 40 nm, and 80 nm gate lengths. Data to the left of line A1 (shown by directional arrow A2) represent reduced spacer widths with increased channel stress for a given dielectric layer stress according to embodiments of the present invention.

0028 It is seen that the ratio of channel stress to dielectric layer stress (vertical axis) increases with reduced spacer width, for example increasing by up to about 60 % at line B1. Therefore, advantageously, an increased level of channel stress can be formed for a given stress level of the dielectric layer following reduced spacer width formation according to embodiments of the present invention. Formation of salicides advantageously further adds to increased channel stress while reducing S/D and SDE region electrical resistance. The increased stress in the channel region together is salicide formation increases charge carrier mobility while reducing short channel effects (SCE) and increasing drive current (I_D) at smaller gate lengths.

0029 Referring back to Figure 2A, is shown another embodiment of the present invention. In this embodiment, the formation steps including formation of two hardmask layers 16A and 16B followed

by removal of the uppermost hardmask layer 16B, and formation of SDE region e.g., 20A and 20B are the same as outlined with respect to the embodiment shown in Figures 1A and 1B.

0030 Still referring to Figure 2A, in the present embodiment, oxide/nitride/oxide spacers are formed of the same preferred materials outlined for the oxide/nitride spacers in the embodiment shown in Figure 1, but additionally including deposition of an uppermost oxide layer to form oxide portion e.g., 18C following conventional wet and/or dry etchback process. The maximum width WB1 of the oxide/nitride/oxide spacers prior to width reduction as measured from the polysilicon or metal electrode 14 sidewall portion is for example, greater than about 450 Angstroms.

0031 Referring to Figure 2B, a conventional oxide wet or dry etching process, preferably an isotropic wet etch process, is first carried out to remove the hardmask layer 16A oxide hardmask layer over the polysilicon electrode 14 as well as removing portions of the spacer oxide portions 18A and 18C. Preferably the oxide portions are removed to a desired reduction in width of the oxide/nitride/oxide spacers e.g., WB1 to WB2. A high dose implant (HDI) process is then carried out to dope the polysilicon

or metal gate electrode 14 as well as forming the S/D regions e.g., 22A and 22B. It will be appreciated that amorphous polysilicon regions may be formed in the polysilicon or metal electrode portion 14 during the HDI process.

0032 Referring to Figure 2C, the nitride portion e.g., 18B of spacer width WB1 is then reduced by a conventional nitride wet or dry etch to form reduced oxide/nitride/oxide spacer width WB2, preferably less than about 500 Angstroms in width, more preferably less than about 400 Angstroms in width, measured at a maximum width of the spacer from the polysilicon or metal gate sidewall. Advantageously, in the spacer thinning process a portion of the underlying SDE region e.g., 20A is exposed, for example an exposed width of the underlying SDE region being about equal to the amount by which the spacer width is Slim.

0033 Referring to Figure 2D, a conventional oxide wet etch process for example a dip in dilute HF is then carried out to remove remaining portions of the oxide portion e.g., 18C of the spacer, including any oxide portions overlying the silicon substrate 10 to form oxide/nitride spacers having substantially vertical sidewall portions e.g., oxide/nitride portions 18A and 18B. A salicide formation process is then preferably carried out

by the same process as previously outlined to form salicide regions e.g., 24A , 24B, and 14A in the same manner as previously outlined in Figure 1E, advantageously extending into a portion of the SDE region e.g., 20A.

0034 Referring to Figure 2E, a stressed dielectric layer 28, optionally including an underlying oxide buffer layer, is then deposited, annealed, and subsequently optionally removed to form a stressed channel region e.g., 26 in the same manner and according to the same preferred embodiments as outlined above for Figure 1F.

0035 Thus, a method for producing reduced width spacers in a CMOS device manufacture process has been presented that allows adjustable control over the width of the spacer prior to forming an overlying stressed dielectric layer and salicide portions. Advantageously, the width of the spacer may be selected to achieve a desired electrical resistance over the S/D and SDE regions as well as achieving a desired increase in compressive or tensile stress in the channel region. The method is cost effective since the number of required steps is limited and the process uses conventional materials and etching processes.

0036 Referring to Figure 4 is a process flow diagram including several embodiments of the present invention. In process 401, a silicon substrate including a CMOS gate structure is provided with SDE doped portions and a double layer hardmask layer overlying the polysilicon or metal electrode portion. In process 403, the uppermost hardmask layer is removed. In process 405, an oxide/nitride or oxide/nitride/oxide spacer is formed. In process 407, the lowermost hardmask layer is removed. In process 409 a high dose implant (HDI) process is carried out to dope the polysilicon layer and form S/D regions. In process 411, the spacers are Slim (width reduced) to a predetermined width according to preferred embodiments. In optional process 413, salicides are formed over S/D regions including SDE regions and the uppermost polysilicon or metal electrode portion. In process 415 a stressed dielectric layer is formed over the CMOS gate structure including Slim spacers. In process 417, an annealing process is carried out to recrystallize amorphous polysilicon or metal electrode portions to create a predetermined stress type (tensile or compressive) and stress level in the channel region underlying the CMOS polysilicon or metal gate structure.

0037 The preferred embodiments, aspects, and features of the invention having been described, it will be apparent to those

skilled in the art that numerous variations, modifications, and substitutions may be made without departing from the spirit of the invention as disclosed and further claimed below.